CLAIMS

1. An integrated circuit, for use as a scheduler of activities to be run on an associated central processor, the circuit being configured to support a "control node" mechanism by incorporating means for holding at least one pair of control variables comprising a "stim-wait" channel corresponding to each of said activities and further incorporating next activity selection logic for identifying those activities which are ready for running on the processor, depending on the status of said control variables.

2. An integrated circuit for use as a scheduler of activities to be run on an associated processor, being of modular structure and constructed from an assembly of tiles, wherein each tile defines a building block having logic and structure, said tiles being abutted one against the other to form a two-dimensional array of n rows and m columns which realises an overall functionality for the integrated circuit and wherein each of the 'n' rows of tiles provides the control logic for each one of 'n' schedulable activities and each of the m columns of tiles provides a particular function.

3. An integrated circuit as claimed in claim 2 comprising a further row of tiles for interfacing with an associated central processor and for generating control signals for said two-dimensional array.

4. An integrated circuit as claimed in claim 2 ~~or 3~~ in which the control logic includes means for holding control variables corresponding to each of said activities and

next-activity selection logic for identifying those activities which are ready for running on the processor, depending on the status of said control variables.

5. An integrated circuit as claimed in claim 4 in which the control variables include at least one "stim-wait" channel.

6. An integrated circuit as claimed in claim 1 ~~or claim 5~~ including means for setting those control variables comprising a "stim-wait" channel in response to a signal received from an associated processor.

7. An integrated circuit as claimed in ~~any of claims 1, 5 or 6~~ Claim 1 including means for setting those control variables comprising a "stim-wait" channel in response to a signal received from an associated peripheral device.

8. An integrated circuit as claimed in ~~any of claims 1, 5, 6 or 7~~ Claim 1 including means for setting those control variables comprising a "stim-wait" channel in response to a signal received from a second integrated circuit as described and claimed herein.

9. An integrated circuit as claimed in ~~any of claims 1 or 4-8~~ Claim 1 including means for temporarily inhibiting any changes to control variables from entering the next- activity-selection logic.

10. An integrated circuit as claimed in ~~any of claims 2 to 9~~ Claim 2 and incorporating decoding and encoding logic for routing signals, identifying one or more of said 'n' activities, between the associated central processor and the appropriate row of tiles.

11. An integrated circuit as claimed in ~~any of claims 1 or 4-10~~ Claim 1 in which the next-activity-selection logic includes means for selecting the next activity to be run on a round robin basis.

12. An integrated circuit as claimed in ~~any of claims 1 or 4-11~~ Claim 1 in which the next activity selection logic includes means for allocating differing priority levels to groups of activities, and for selecting the next activity to run within a group on a round robin basis within that group.

13. An integrated circuit as claimed in ~~any preceding claim~~ Claim 1 and including means for detecting when a schedulable activity has a higher priority than that activity currently running on an associated central processor and thereby generating an interrupt signal.

14. An integrated circuit as claimed in ~~any preceding claim~~ Claim 1 and incorporating a counter circuit.

15. An integrated circuit as claimed in ~~any preceding claim~~ Claim 1 configured for asynchronous operation, by incorporating level-driven, clock-free ripple logic.

16. An integrated circuit as claimed in ~~any preceding claim~~ Claim 1 and being fabricated using CMOS techniques.

17. A processing network comprising a central processing unit for running a plurality of activities and a scheduler of activities linked to the processing unit via a data bus in which said scheduler comprises an integrating circuit in accordance with ~~any of the preceding claims~~ Claim 1.

18. A processing network comprising a control processing unit for running a plurality of activities, a

scheduler of activities and a peripheral device, in which said scheduler comprises an integrating circuit in accordance with ~~any of claims 1 or 5-17~~ claim 1 and in which the scheduler further includes means for setting at those control variables comprising a "stim-wait" channel in response to a signal received from said peripheral device.

19. A multiprocessor network comprising a plurality of central processing units, each being linked to an associated scheduler and each scheduler being linked to adjacent schedulers in which each of said schedulers comprises an integrating circuit in accordance with ~~any of claims 1 or 5-17~~ claim 1.

20. A multiprocessor network as claimed in claim ~~20~~ 19 in which at least one of said schedulers includes means for setting those control variables comprising a "stim-wait" channel in response to a signal received from an adjacent scheduler.

21. A multiprocessor network as claimed in either of claims 20 ~~or 21~~ and further including a peripheral device linked to a scheduler, in which the scheduler includes means for setting those control variables comprising a "stim-wait" channel in response to a signal received from said peripheral device.